UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,914	09/27/2001	Sehat Sutardja	MP0115	5719

23624 7590 04/14/2004

MARVELL SEMICONDUCTOR, INC.
INTELLECTUAL PROPERTY DEPARTMENT
700 FIRST AVENUE, MS# 509
SUNNYVALE, CA 94089

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/14/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,914	SUTARDJA	
	Examiner	Art Unit	
	Alexander O Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,8,11-16,19,20,22-25 and 27-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,8,11-16,19,20,22-25 and 27-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/21/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 09/966914 Attorney's Docket #: MP0115

Filing Date: 9/27/01;

Applicant: Sutardja

Examiner: Alexander Williams

Applicant's Amendment, filed 1/16/04 is acknowledged.

Claims 5, 6, 9, 10, 17, 18, 21 and 26 have been canceled.

The disclosure is objected to because of the following informalities: The divisional application information should be updated.

Appropriate correction is required.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 to 4, 7, 8, 11 to 16, 19, 20 and 22 to 30 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shiraishi et al. (U.S. Patent # 6,525,414 B1) in view of Kato et al. (U.S. Patent # 5,424,573).

For example, in claim 1, similar claims 21, 29 (claim 1 and 12) and 30 which is similar to claim 29) and method of forming integrated chip package in claim 13, Shiraishi et al. **(figure 4)** show an integrated chip package, comprising: at least one semiconductor chip **101,103** each having a first surface and a second surface; an intermediate substrate **107** electrically coupled via conductive bumps **110** to the first surface of the at least one semiconductor chip; a planar package substrate **112** having a first surface electrically coupled to the intermediate substrate via a plurality of bonding wires **114**, the intermediate substrate arranged above and spaced apart

(with 105 and the lower portion of 111 between 107 and 112) from the planar package substrate, but fail to explicitly show a heat sink having side portions extending towards the planar package surface, the heat sink thermally coupled to the second surfaces of the semiconductor chips so that heat generated from the at least one semiconductor chip flows toward the heat sink.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on (a frame 82 connected to a lid 83) and a heat sink; and intermediate substrate and board and semiconductor chip deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Therefore, it would have been obvious to one of ordinary skill in the art to use the frame with the lid and the heat sink; and intermediate substrate and board and semiconductor chip as

"merely a matter of obvious engineering choice" as set forth in the above case law.

Kato et al. Is cited for showing a semiconductor package having optical interconnection access. Specifically, Kato et al. (figure 2) discloses at least two semiconductor chips **10** each having a first surface and a second surface and a heat sink **82,83** having side portions extending towards the planar package **80** surface, the heat sink thermally coupled to the second surfaces of the semiconductor chips so that heat generated from the at least two semiconductor chip flows toward the heat sink **(see column 7, lines 47-58)** for the purpose of providing means which achieves practical application of optical interconnection technology to high speed and/or high density semiconductor package the bottleneck with regard to input/output pins in high speed and/or high density semiconductor packages.

In claims 2, 14 and similar claim 23, the combination with Kato et al.'s second surface of the at least one semiconductor chip **10** is adhesively bonded to the heat sink **82,83**.

In claims 3, 15 and similar claim 24, the combination with Kato et al.'s heat sink **82,83** is substantially thermally isolated from the planar package substrate **80**.

In claims 4, 16, and similar claim 25, the combination with Shiraishi et al.'s intermediate substrate **107,105** formed from a material selected from silicon **105**.

In claim 7, the combination with Shiraishi et al.'s conductive bumps **110** formed form Au.

In claim 8 and 19, the combination with Shiraishi et al.'s intermediate substrate **107** includes a circuit plane **108** selected from interconnect planes.

In claims 11, 20 and similar claim 28, the combination show either reference with planar package substrate including conductive pads on a second surface **(bottom of 112)**.

In claim 12, the combination with Shiraishi et al. further comprising a support material **(with 105 and the lower portion of 111 between 107 and 112)** arranged between the planar package **112** and the intermediate substrate **107**.

In claim 27, the combination with Shiraishi et al.'s flip chip conversion means **107** including a means for electrically interconnecting (by 109).

Therefore, it would have been obvious to one of ordinary skill in the art to use Kato et al.'s two semiconductor chips to modify Shiraishi et al.'s package of one semiconductor chip for the purpose of providing means which achieves practical application of optical interconnection

technology to high speed and/or high density semiconductor package the bottleneck with regard to input/output pins in high speed and/or high density semiconductor packages.

Response

Applicant's arguments filed 1/16/04 have been fully considered, but are moot in view of the new grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,778,737,738,734,712,704,710,717, 720,532,724,728,725,528	3/17/03 11/3/03 4/12/04
Other Documentation: foreign patents and literature in 257/686,685,723,777,778,737,738,734,712,704,710,717, 720,532,724,728,725,528	3/17/03 11/2/03 4/12/04
Electronic data base(s): U.S. Patents EAST	3/17/03 11/2/03 4/12/04

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AOW
4/12/04

Alexander Williams
Primary Examiner